ABSTRACT

A process sequence for forming a MOSFET device featuring a high k gate insulator layer, wherein the use of the high k gate insulator layer requires no additional photolithographic procedures, has been developed. After deposition of a high k gate insulator layer followed by the definition of an overlying conductive gate structure, an insulator layer is deposited. An anisotropic dry etch procedure is then employed to first define offset insulator spacers on the sides of the conductive gate structure, then to selectively remove the unwanted portions of the high k gate insulator layer. The use of the high k gate insulator layer provides a thin gate insulator layer with less risk of leakage when compared to counterpart gate insulator layers such as silicon dioxide, while the integration of the definition of the offset insulator spacer step and of the high k gate layer removal procedure, results in fabrication cost savings.